FIG. 1 *basic power delivery system*

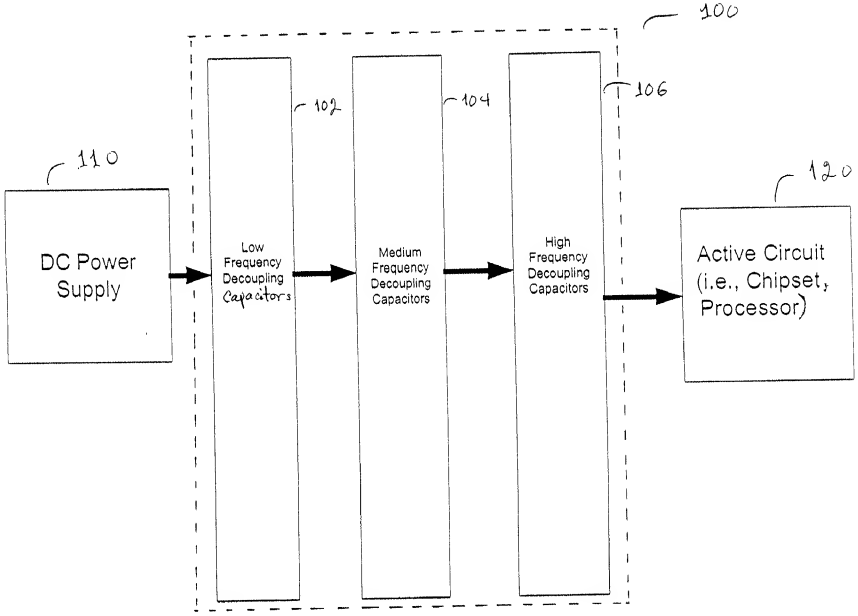

FIG. 2

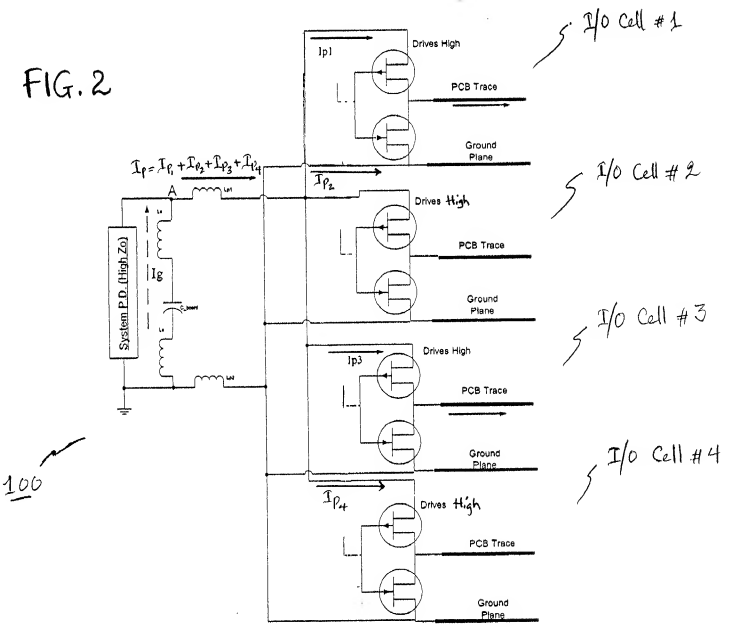
I/O Cell #1
I/O Cell #2
I/O Cell #3
I/O Cell #4
Ipl
Drives High
PCB Trace
Ground Plane
$I_p = I_{p_1} + I_{p_2} + I_{p_3} + I_{p_4}$
A
I_{p_2}
Drives High
PCB Trace
Ground Plane
System P.D. (High Zo)
Ig
Ip3
Drives High
PCB Trace
Ground Plane
I_{p_4}
Drives High
PCB Trace
Ground Plane
100

FIG. 3

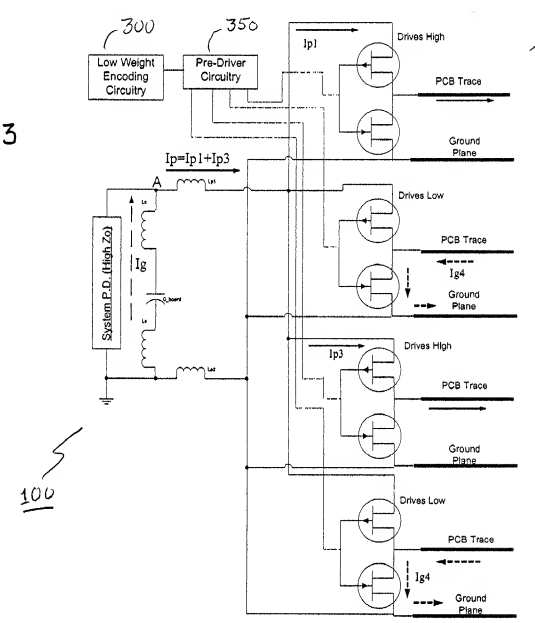
300
Low Weight Encoding Circuitry
350
Pre-Driver Circuitry
Ip1
Drives High
PCB Trace
Ground Plane
I/O Cell #1
Ip=Ip1+Ip3
Drives Low
PCB Trace
Ig4
Ground Plane
I/O Cell #2
System P.D. (High Zo)
Ig
Ip3
Drives High
PCB Trace
Ground Plane
I/O Cell #3
Drives Low
PCB Trace
Ig4
Ground Plane
I/O Cell #4
100

FIG. 4

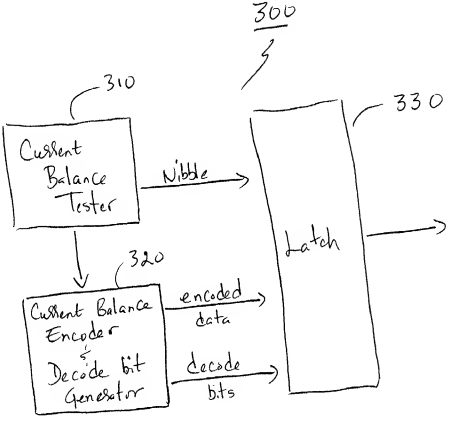
300
310
330
Current Balance Tester
Nibble
Latch
320
Current Balance Encoder & Decode bit Generator
encoded data
decode bits

FIG. 5

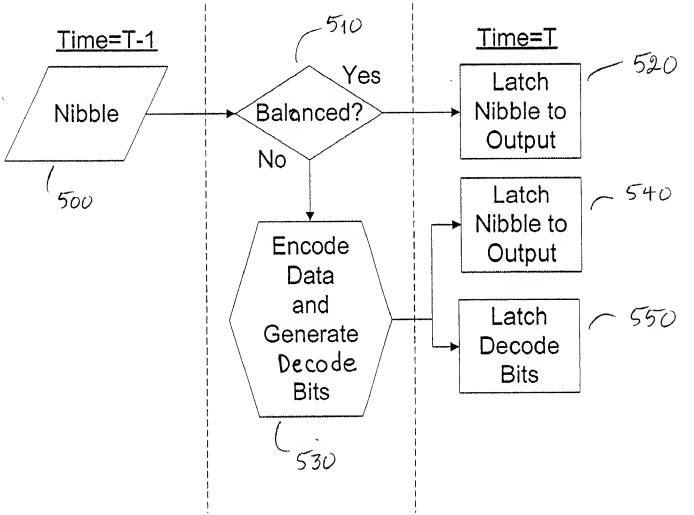
Time=T-1
Nibble
500
510
Balanced?
Yes
No
Time=T
Latch Nibble to Output
520
Latch Nibble to Output
540
Encode Data and Generate Decode Bits
530
Latch Decode Bits
550

FIG. 6A

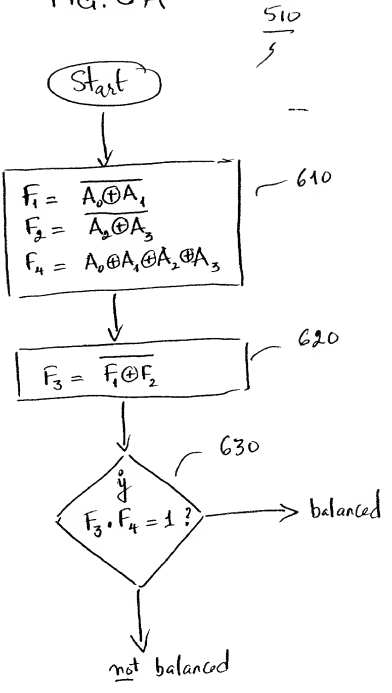
510
Start
$F_1 = \overline{A_0 \oplus A_1}$
$F_2 = \overline{A_2 \oplus A_3}$
$F_4 = A_0 \oplus A_1 \oplus A_2 \oplus A_3$
610
$F_3 = \overline{F_1 \oplus F_2}$
620
630
$F_3 \cdot F_4 = 1$?
y
balanced
not balanced

FIG. 7A

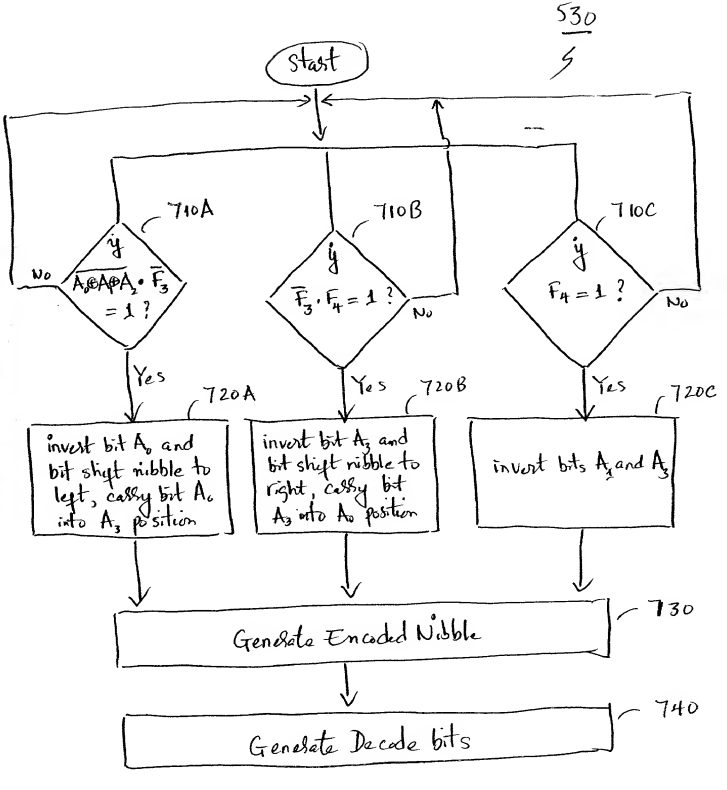
530
Start
710A
$\overline{A_3 \oplus A_2 \oplus A_1} \cdot \overline{F_3} = 1$?
No
Yes
710B
$\overline{F_3} \cdot F_4 = 1$?
No
Yes
710C
$F_4 = 1$?
No
Yes
720A
invert bit A_0 and bit shift nibble to left, carry bit A_0 into A_3 position
720B
invert bit A_3 and bit shift nibble to right, carry bit A_3 into A_0 position
720C
invert bits A_2 and A_3
730
Generate Encoded Nibble
740
Generate Decode bits

FIG. 6B – TABLE #1

A_0	A_1	A_2	A_3	F_1	F_2	F_3	F_4	$F_3 \bullet F_4$	
0	0	0	0	1	1	1	0	0	
0	0	0	1	1	0	0	1	0	
0	0	1	0	1	0	0	1	0	
0	0	1	1	1	1	1	1	1	Balanced
0	1	0	0	1	0	0	1	0	
0	1	0	1	0	0	1	1	1	Balanced
0	1	1	0	0	0	1	1	1	Balanced
0	1	1	1	0	1	0	1	0	
1	0	0	0	0	1	0	1	0	
1	0	0	1	0	0	1	1	1	Balanced
1	0	1	0	0	0	1	1	1	Balanced
1	0	1	1	0	1	0	1	0	
1	1	0	0	0	1	1	1	1	Balanced
1	1	0	1	1	0	0	1	0	
1	1	1	0	1	0	0	1	0	
1	1	1	1	1	1	1	0	0	

FIG. 7B - TABLE #2

							Encoded Nibble				Decode Bits	
A0	A1	A2	A3	Right Shift	Left Shift	Invert	A0	A1	A2	A3		
0	0	0	0			x	0	1	0	1	1	1
0	0	0	1		x		0	0	1	1	1	0
0	0	1	0	x			1	0	0	1	0	1
0	1	0	0	x			1	0	1	0	0	1
0	1	1	1	x			0	0	1	1	0	1
1	0	0	0	x			1	1	0	0	0	1
1	0	1	1	x			0	1	0	1	0	1
1	1	0	1	x			0	1	1	0	0	1
1	1	1	0		x		1	1	0	0	1	0
1	1	1	1			x	1	0	1	0	1	1